solutions available at http://mathieu.delalandre.free.fr/teachings/operating1.html

Partie 1

scheduling		buffer	ww bits		C state	P state
Process	Code		P	C		
		5	0	0	awake	sleepy
C	1,3,4,5	4	0	0	awake	awake
P	3	5	0	0	awake	awake
C	1	5	0	0	awake	awake
P	4,1	5	0	0	awake	awake
C	3,4,5	4	1	0	awake	awake
P	2,3,4	5	0	0	awake	awake
C	1	5	0	0	awake	awake
P	1,2	5	0	0	awake	sleepy

scheduling		buffer	fill		empty		C state	P state	
Process	Code		value	Q	value	Q			
		0	0	C	2	∅	blocked	ready	
P	1,2,3	1		∅	1		ready	ready	P fills the buffer and wakeups C
P	1,2,3,1	2	1		0	P		blocked	P fills the buffer and blocks on empty
C	2,3	1				∅		ready	C restarts, pops the buffer and wakeups P
P	2,3,1	2	2			P		blocked	P restarts, fills the buffer and blocks on empty
C	1,2,3	1	1			∅		ready	C pops the buffer and wakeups the consumer
C	1,2,3,1	0	0	C	1		blocked		C continues to pop the buffer, and blocks on fill
P	2,3	1		∅			ready		P restarts, fills the buffer and wakeups C

Partie 2

scheduling		buffer	fill		empty		mutex			
Process	Code		value	Q	value	Q	value	Q	Section	
		4	4	∅	1	∅	false	∅	∅	
P	1,2,3,4,5,1	5	5	∅	0	P	false	∅	∅	P fills the buffer and blocks
C2	1,2	5	4	∅	0	P	true	∅	C2	C2 accesses the buffer and locks the mutex
C1	1,2	5	3	∅	0	P	true	C1	C2	C1 blocked when accessing the mutex
C2	3,4,5	4	3	∅	0	∅	true	∅	C1	C2 frees the mutex, unblocks C1 and P
P	2	4	3	∅	0	∅	true	P	C1	P blocks on the mutex
C2	1,2	4	2	∅	0	∅	true	C2,P	C1	C2 blocks on the mutex
C1	3,4	3	2	∅	0	∅	true	C2	P	C1 restarts and frees P
P	3,4	4	2	∅	0	∅	true	∅	C2	P restarts and frees C2
C2	3	3	2	∅	0	∅	true	∅	C2	C2 restarts and pops the buffer
P	5	3	3	∅	0	∅	true	∅	C2	P ups fill
C1	5	3	3	∅	1	∅	true	∅	C2	C1 ups empty
C2	4,5	3	3	∅	2	∅	false	∅	∅	C2 frees the mutex and ups empty

scheduling		buffer	count	Conditions		Section	entry queue
Process	Code			full	empty		
		2	2	P2	∅	∅	∅
C2	0,1,3,4	1	1	P2	∅	C2	∅
C1	0	1	1	P2	∅	C2	C1
P1	0	1	1	P2	∅	C2	P1,C1
P3	0	1	1	P2	∅	C2	P3,P1,C1
C2	5,0	1	1	∅	∅	C2-∅	C2,P2,P3,P1,C1
C1	1,3,4,5,0	0	0	∅	∅	C1-∅	C1,C2,P2,P3,P1
P1	1,3,4,5,0	1	1	∅	∅	P1-∅	P1,C1,C2,P2,P3
P3	1,3,4,5,0	2	2	∅	∅	P3-∅	P3,P1,C1,C2,P2
P2	1,2	2	2	P2	∅	P2-∅	P3,P1,C1,C2
C2	1,3,4,5	1	1	∅	∅	C2-∅	P2,P3,P1,C1
C1	1,3,4,5,0	0	0	∅	∅	C1-∅	C1,P2,P3,P1
C2	0	0	0	∅	∅	∅	C2,C1,P2,P3,P1

scheduling		buffer	count	Conditions			Section	entry queue	Turn
Process	Code			full	empty	signal			
		2	2	P2	∅	∅	∅	∅	∅
C2	0,1,3,4	1	1	P2	∅	∅	C2	∅	Enter 1
C1	0	1	1	P2	∅	∅	C2	C1	Enter 1
P1	0	1	1	P2	∅	∅	C2	P1,C1	Enter 1
P3	0	1	1	P2	∅	∅	C2	P3,P1,C1	Enter 1
C2	5	1	1	∅	∅	C2	C2-P2	P3,P1,C1	Enter 1
P2	3,4,5,0	2	2	∅	∅	C2	P2-∅	P2,P3,P1,C1	Signalled
C1	1,3,4,5,0	1	1	∅	∅	C2	C1-∅	C1,P2,P3,P1	Enter 2
P1	1,3,4,5,0	2	2	∅	∅	C2	P1-∅	P1,C1,P2,P3	Enter 3
P3	1,2	2	2	P3	∅	C2	P3-∅	P1,C1,P2	Enter 4
C2	1,3,4,5	1	1	∅	∅	C2-C2	C2-P3	P1,C1,P2	Signal 5
P3	3,4,5,0	2	2	∅	∅	C2	P3-∅	P3,P1,C1,P2	Signalled
P2	1,2	2	2	P2	∅	C2	P2-∅	P3,P1,C1	Enter 1